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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/829,320	04/21/2004	Tomomi Momohara	81790.0312	5681

26021 7590 05/24/2005

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EXAMINER	
FENTY, JESSE A	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 05/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/829,320	MOMOHARA, TOMOMI	
	Examiner	Art Unit	
	Jesse A. Fenty	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *20-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20-25 and 32-35* is/are rejected.

7)☒ Claim(s) *26-31,36 and 37* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/14/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 20-25 and 32-35 are rejected under 35 U.S.C. 102(b) as being anticipated by Fujita et al. (U.S. Patent No. 5,336,915).

In re claims 20 and 32, Fujita (Figs. 1-7) discloses a semiconductor device comprising:

A semiconductor substrate (10) of a first conductivity type;

A first well (14) of a second conductive type provided in the semiconductor substrate;

A second well (18) of the first conductive type provided in the first well;

A third well (12) of the second conductive type provided in the semiconductor substrate;

A fourth well (16) of the first conductive type provided in the third well;

Semiconductor elements (22-3, 22-4, 20-3, 20-4) provided in the first and second wells, the semiconductor elements constructing a first functional integrated circuit (analog circuit);

Semiconductor elements (22-1, 22-2, 20-1, 20-2) provided in the third and fourth wells, the semiconductor elements constructing a second functional integrated circuit (digital circuit);

A first internal power source voltage generating circuit (51) provided in the first well, the first internal power source voltage generating circuit configured to generate a first internal power source voltage being applied to the first functional integrated circuit; and

A second internal power source voltage generating circuit (84) provided in the third well, the second internal power source voltage generating circuit configured to generate a second internal power source voltage being applied to the second functional integrated circuit.

In re claims 21 and 33, Fujita (Figs. 4, 5) discloses the devices of claims 20 and 32 respectively, wherein each of the first and second functional integrated circuits has a dedicated output (63, 74) terminal for outputting an output signal when a potential is applied to the potential application terminal thereof.

In re claim 22, Fujita (Fig. 6) discloses the device of claim 20, further comprising:

A first controlling circuit (Vcc1) provided in the first well and configured to control the first internal power source voltage generating circuit based on an inputted first control signal; and

A second controlling circuit (Vcc2) provided in the third well and configured to control the second internal power source voltage generating circuit based on an inputted second control signal.

In re claim 23, Fujita (Fig. 1) discloses the device of claim 20, wherein the first internal power source voltage generating circuit generates the first internal power source voltage according to an external power source voltage (Vcc1), and the second internal power source voltage generating circuit generates the second internal power source voltage according to the first inter first internal power source voltage.

In re claims 24 and 35, Fujita (Figs. 4, 5) discloses the devices of claims 23 and 34, further comprising:

A first controlling circuit (51 and Comp) provided in the first well and configured to control the first internal power source voltage generating circuit which turned-on and turned-off (via switches 72-1 – 72-256) generating the first internal power source voltage based on an inputted first signal;

A second controlling circuit provided in the third well and configured to control the second internal power source voltage generating circuit which turned-on and turned-off (via switches 81-1 – 81-256) generating the second internal power source voltage based on an inputted second control signal.

In re claim 25, Fujita discloses the device of claim 20, wherein the first functional integrated circuit and the second functional integrated circuit each include an analog and a digital circuit.

In re claim 34, Fujita discloses the device of claim 32, wherein the internal power source voltage generating circuit generates the first and second internal power source voltages according to an external power source voltage (Vcc1).

In re claim 35, Fujita discloses the device of claim 34, further comprising:

a controlling circuit provided in the first well and configured to control the internal power source voltage generating circuit which turned-on and turned-off generating the first internal power source voltage based on an inputted first control signal, and configured to control the second internal power source voltage generating circuit which turned-on and turned-off generating the second internal power source voltage based on an inputted second control signal.

Allowable Subject Matter

3. Claims 26-31 and 36-39 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

4. Applicant's arguments filed 01/25/05 have been fully considered but they are not persuasive.

a. Applicant argues that the regions (51) and (84) of Fujita et al. (U.S. Patent No. 5,336,915) are not power source generating circuits. However, referring to Figs. 1-5, examiner asserts that the structure of the claims is no different than the structure of the prior art Fujita. The power source generating circuits of the instant claims are not described in detail in the pending claims. Looking to the specification (sections [0167] and [0168] of the pre-grant pub version, for better reference0, the power source generating circuits (30-3 and 30-4) of the instant application are nothing more than FET devices configured in a particular manner in the wells (22-3 and 22-4). As claimed, regarding the structure, Fujita provides the same well regions and semiconductor element regions as the instant claims. The power source generating circuits, as understood, are little more than intended use variations of the semiconductor FET devices. Therefore, the sample and hold circuit (51) and the switch control logic circuit (80, 84) noted in the Non-Final Rejection are just different manifestations of power source generating circuits

that are constructed by the same element regions as the claimed components. The non-final rejection therefore stands.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 571-272-1729. The examiner can normally be reached on 5/4-9 1st Fri. Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jesse A. Fenty
Examiner
Art Unit 2815

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER